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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,972	07/30/2001	Richard D. Taylor	10010393	9408

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EXAMINER	
CHUNG, PHUNG M	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
08/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/917,972	TAYLOR ET AL.	
	Examiner	Art Unit	
	Phung My Chung	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 9-15 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-6, 9-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mates (6,564,347).

As per claims 1-3 and 6, Mates discloses an integrated circuit comprising:

a processing core (processor);

an internal memory containing test routines that the processing core executes to test the integrated circuit; and

an interface coupled to the processing core to permit activation of a first output signal indicating a test result from executing the test routines. (See Fig. 2, col. 2, lines

25-29, col. 4, lines 26-34 and col. 7, line 61 to col. 8, line 8). Wherein the internal memory contains a first set of test routines for execution during a production test of the integrated circuit (integrated circuit manufactures test, col. 7, lines 54-60) and a second set of test routines for execution during an in-product test of the integrated circuit (after manufacture of the integrated circuit to be test, col. 2, lines 67-68). Mates does not specifically disclose wherein a control input to the integrated circuit controls whether the first or second set of routines are executed. However, Mates discloses (a first test routine) the test routine is executed during production test (integrated manufacture, col. 7, lines 54-60). Mates col. 2, lines 67-68 discloses (a second test routine, an in-product test of the integrated circuit) the test routines can be added after manufacture of the integrated circuit to be tested, and Mates discloses a programmable logic analyzer unit (LAU) embedded within an integrated circuit. This programmable LAU tests a function of the integrated circuit (col. 2, lines 27-28). Variety of available signal types provides the LAU with flexibility in terms of the types of test that can be performed (col. 7, lines 10-22). Therefore, it would have been obvious to a person of skilled in the art, at the time the invention was made, base on these teaching of Mates to provide a first set of test routines for execution during a production test of the integrated circuit and a second set of test routines for execution during an in-product test of the integrated circuit and a control signal input to the integrated circuit to control whether the first or second set of routines are executed. With these built-in test routines, the testers may be able to realize a significant savings related to test equipment by obviating a need for costly,

external logic analyzers. As a need for external logic analyzers is reduced, so are the costs associated with maintenance repair. (See col. 7, lines 54-60).

As per claim 5, Mates further discloses wherein the processing core executes the test routines from the internal memory during a production test of the integrated circuit (integrated circuit manufacture test, col. 7, lines 54-60).

As per claims 9-13, 15 and 17, Mate disclose a method for an integrated circuit, comprising:

using a processing core in the integrated circuit to execute test routines stored in the integrated circuit; and

observing a first signal output from the integrated circuit as a result of the processing core executing the test routines, the first signal indicating whether the execution of the test routines detected a failure in the integrated circuit. (See Fig. 2, col. 2, lines 25-29, col. 4, lines 26-34 and col. 7, line 61 to col. 8, line 8). Mate does not specifically disclose:

applying a control signal to the integrated circuit; and

selecting the test routines according to the control signal. However, Mates discloses (a first test routine) the test routine is executed during production test (integrated manufacture, col. 7, lines 54-60). Mates col. 2, lines 67-68 discloses (a second test routine, an in-product test of the integrated circuit) the test routines can be added after manufacture of the integrated circuit to be tested, and Mates discloses a programmable logic analyzer unit (LAU) embedded within an integrated circuit. This programmable LAU tests a function of the integrated circuit (col. 2, lines 27-28). Variety

of available signal types provides the LAU with flexibility in terms of the types of test that can be performed (col. 7, lines 10-22). Therefore, it would have been obvious to a person of skilled in the art, at the time the invention was made, base on these teaching of Mates to provide a first set of test routines for execution during a production test of the integrated circuit and a second set of test routines for execution during an in-product test of the integrated circuit and a control signal input to the integrated circuit to control whether the first or second set of routines are executed. With these built-in test routines, the testers may be able to realize a significant savings related to test equipment by obviating a need for costly, external logic analyzers. As a need for external logic analyzers is reduced, so are the costs associated with maintenance repair. (See col. 7, lines 54-60).

As per claim 14, Mates further discloses wherein the test method is performed during production of the integrated circuit (integrated circuit manufacture test, col. 7, lines 54-60).

3. Applicant's arguments filed 5/17/07 have been fully considered but they are not persuasive because:

Applicant argues that Mates does not disclose or teach the limitation of claims 1 and 9. therefore, these claims have been amended to include the limitation of claims 8, "wherein a control signal input to the integrated circuit controls whether the first or second set of routines are executed" and claim 16, "applying a control signal to the integrated circuit; and selecting the test routines according to the control signal".

Examiner disagrees with applicant because Mates does not specifically disclose wherein a control input to the integrated circuit controls whether the first or second set of routines are executed. However, Mates discloses (a first test routine) the test routine is executed during production test (integrated manufacture, col. 7, lines 54-60). Mates col. 2, lines 67-68 discloses (a second test routine, an in-product test of the integrated circuit) the test routines can be added after manufacture of the integrated circuit to be tested, and Mates discloses a programmable logic analyzer unit (LAU) embedded within an integrated circuit. This programmable LAU tests a function of the integrated circuit (col. 2, lines 27-28). Variety of available signal types provides the LAU with flexibility in terms of the types of test that can be performed (col. 7, lines 10-22). Therefore, it would have been obvious to a person of skilled in the art, at the time the invention was made, base on these teaching of Mates to provide a first set of test routines for execution during a production test of the integrated circuit and a second set of test routines for execution during an in-product test of the integrated circuit and a control signal input to the integrated circuit to control whether the first or second set of routines are executed. With these built-in test routines, the testers may be able to realize a significant savings related to test equipment by obviating a need for costly, external logic analyzers. As a need for external logic analyzers is reduced, so are the costs associated with maintenance repair. (See col. 7, lines 54-60).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phung My Chung
Primary Patent Examiner
Art Unit 2117